SDS

MODULE DATA SHEET

HIGH SPEED MEMORY

FT40

ASSY NO. 132700

DESCRIPTION

The FT40 high-speed memory module provides economical, fast-access storage of 128 bits on one module, arranged as sixteen 8-bit bytes. Read time is 110 nanoseconds or less. Write time is 125 nanoseconds or less. The module contains sixteen identical large-scale integrated circuits (SDS 304) which combine storage with address and driving functions. Each IC has 178 components on a single 104 by 95 mil chip, comprising eight flip-flops, 3-bit address decoding and control, input and output buffers, and power gating. The latter feature removes 60% of power from non-addressed circuits without affecting data. Additional address logic and input buffering external to the 304 ICs is provided on the module.

The FT40 is particularly useful in scratchpads. These are small, decentralized high speed memories recently made feasible by the advent of large-scale integration (LSI). Cost per bit lies between the costs associated with core memories and those of IC flip-flop registers.

The IC scratchpad performs significantly faster than the core memory. Typical core access time is greater than 700 nanoseconds while the FT40 cycle is 125 nanoseconds or less. Because the FT40 interfaces directly with other modules in the T Series module line it eliminates special read/write electronics and power supplies normally required by core memories. Therefore the module is particularly attractive for small memory systems.

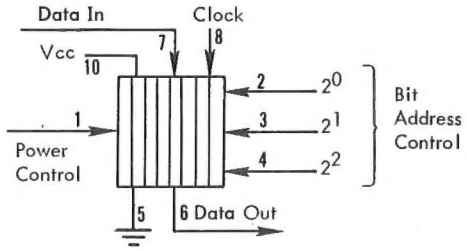
The scratchpad significantly betters the cost per bit of flip-flop storage by a ratio of about 3 to 1. Thus the FT40 furnishes high speed buffer storage at relatively low cost.

The FT40 is extremely convenient to use because inputs and outputs have standard T Series input gating and output buffering. Readout is non-destructive. Writing is simple, requiring only address, Clock, and data.

CIRCUIT DESCRIPTION AND OPERATION

Operation of the SDS 304 IC*

The integrated circuit stores eight bits. It is symbolized as shown below by a square with eight divisions. Data is written in or read out one bit at a time, using the storage position (flip-flop) that is chosen by the three lowest order address lines (2^0, 2^1, 2^2).



A read operation requires that Power Control be True (+4v) and that Clock remain False (0v). All controls on the IC must be stable for 75 nsec before reliable data is available at the IC output, pin 6. Timing requirements for the module are somewhat different because of the additional delay through the data and address buffers, as described later.

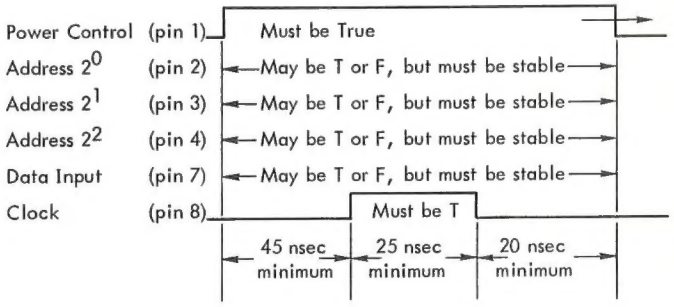
*For additional description of the IC as well as computer applications of the module refer to "Integrated Scratch Pads Sire New Generation of Computers," by J. Mendelson, G. Potter, and S. Sirkin, Electronics, McGraw-Hill, April 4, 1966. Reprint available from SDS.

SPECIFICATIONS, FT40 MODULE

Maximum Operating Frequency	10 Mc (typical)
Input Logic Levels	Logic 1: +4V Logic 0: 0V
Output Logic Levels	Logic 1: +4V Logic 0: 0V
Fan-out (each output)	11 Unit loads (42 ma) with pull-up resistor connected.
Load imposed by each logic input	pins 20, 21, 22, 26, 27: 2 unit loads; all others 1 unit load.
Circuit Delay	Read: 110 nsec worst case (60 nsec typical) Write: 165 nsec worst case (90 nsec typical)
Write Control Conditions (worst case)	Address, Data, and Write-enable should be stable 80 nsec before clock leading edge, and remain stable 45 nsec after clock trailing edge. Minimum clock pulse: 40 nsec.
Read Control Conditions	Address should be stable 110 nsec before outputs are read.
+4 Volt Supply	1.28 amp max. (550 ma typical)
+8 Volt Supply	146 ma max. (63 ma typical)
-8 Volt Supply	2 ma
Module Dissipation	6.25 watts max. (2.7 watts typical)
Temperature Range	+5°C to +50°C with convection cooling +5°C to +70°C with forced air cooling, 100 linear lpm airflow (use ZT20)

A write operation requires that Power Control be True, that Data Input (pin 7) be stable, and that the address lines also be stable, for 45 nsec prior to the time the Clock input goes True. Clock must remain True 25 nsec minimum. Following the Clock falling edge, Power Control, Data, and Address lines must remain stable for an additional 20 nsec. Written data becomes available during a write cycle at the Data Output (pin 6) 50 nsec after Clock falling edge, if address is not changed. Note that these figures do not include delays due to buffers on the module.

Write cycle timing relationships for the SDS 304 IC are summarized below:



Note that when Power Control is False, IC output is True.

Organization of SDS 304 ICs on Module

Sixteen of the 304 ICs are placed on the FT40 module, arranged in two columns, as shown on the logic diagram. When the module is addressed (bits 2^4 through 2^8 all True) one of the two columns of ICs is activated by the output of one of the two column-control buffers, which places +4v on all the IC Power Control inputs in its column. The other control buffer output must be held at 0. The appropriate column is chosen by the 2^3 and $\overline{2^3}$ address bits, at least one of which must be False to prevent damage to the module.

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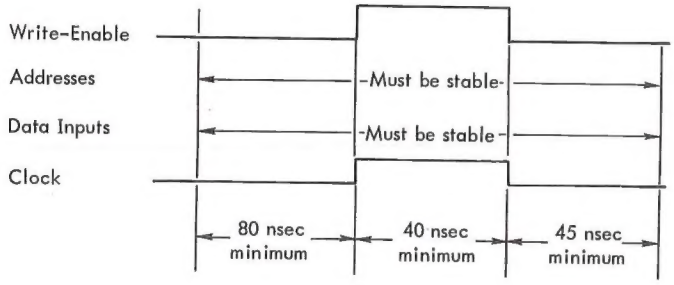
Pairs of IC data inputs are connected as shown, preceded by data buffers which improve noise rejection and decrease load on the input lines. Pairs of outputs are also bussed, forming a wired-AND function; that is, if either output goes False (0v) the output of the bus is False, while if both outputs are True the bus is True. As mentioned the output of a 304 IC is always True when it is deactivated, that is, when its Power Control input is False. Therefore the outputs of one column (the deactivated column) are all True so that the outputs of the other (activated) column determine states of the data output buses.

Note that the eight bits which are simultaneously available at the data output buses originate in eight 304 ICs, one bit from each IC in a column. These eight bits taken in parallel constitute a "byte". A possible point of confusion arises from the fact that each IC contains 8 bits, and it is easy to make the mistake of thinking that the 8-bit byte originates from one IC. This is incorrect because only one bit at a time is available from a 304 IC, as chosen by the three lowest order address bits, 2^0, 2^1, and 2^2.

Module Timing

Worst case module timing requirements differ from the IC timing requirements given previously because the additional buffer circuitry on the module may introduce delay skew or pulse narrowing of the Clock pulse. Delay skew is the difference in delay between the buffer with the longest delay and the buffer with the shortest delay. Pulse narrowing is the change in pulse length that can result when a pulse passes through a buffer whose turn-on time differs from turn-off time. These factors may also vary with temperature and power supply variations.

The write-cycle timing diagram below gives settling times and Clock width which contain a safety factor for worst case conditions.

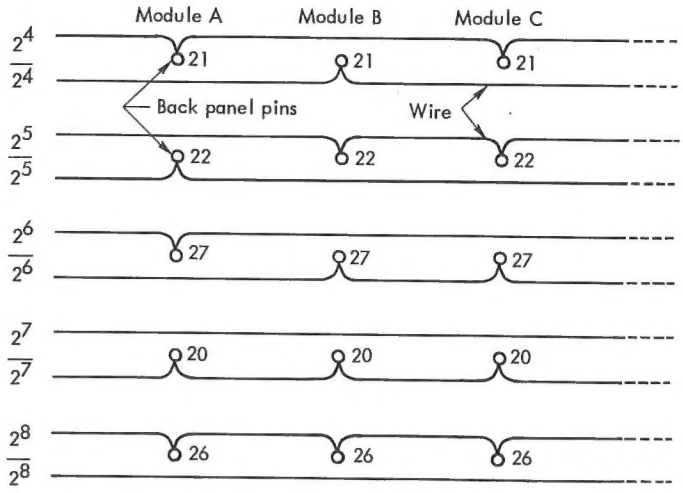


Written data becomes available during a write cycle for reading at the Data Output buses within 80 nsec or less after Clock falling edge. During a read-only operation, data is reliably available 110 nsec after control signals have stabilized.

Organization of Several Modules into Scratchpad Memory; Use of Module Address

A single FT40 module stores 128 bits: eight 8-bit bytes (64 bits) from each of two columns of ICs. The address logic is sufficient to connect as many as thirty-two FT40 modules together into a memory which has eight parallel data output buses and a maximum of 16 x 32 = 512 addresses. This provides eight 8-bit bytes from each of up to 64 columns (32 modules) of ICs, yielding convenient storage for up to 512 bytes, or 4096 bits. The bytes can be extended to 16-bit half-words, 32 bit words, or more by simply wiring additional groups of modules in parallel using the same 512 addresses. Addresses can also be expanded with external logic.

The address lines 2^4 through 2^8 activate one module of the group; the desired byte of that module is addressed using address bits 2^0, 2^1, 2^2, and 2^3, $\overline{2^3}$. Ten address lines are required on the back panel, but etched wiring for both phases of the 2^0, 2^1, 2^2, and 2^4 through 2^8 lines is not provided on the card, since the proper distribution of address signals can be made on the back panel as shown in the example at right above (addresses shown are arbitrary). Both phases of the 2^3 address must be connected to each module, however.

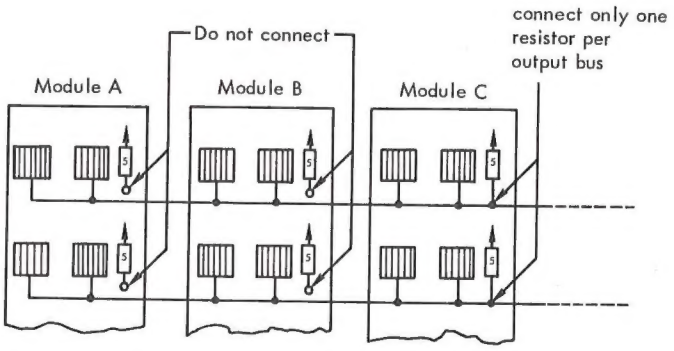


	Module Address	Module Address	Module Address
2^4:	1	0	1
2^5:	0	1	1
2^6:	1	0	0
2^7:	0	0	0
2^8:	1	1	1

When the lines are run in such a way that each module has a unique address, all IC outputs except those of the addressed module and column are predictably at logical 1 (True). Therefore the data output buses assume the states of the addressed outputs.

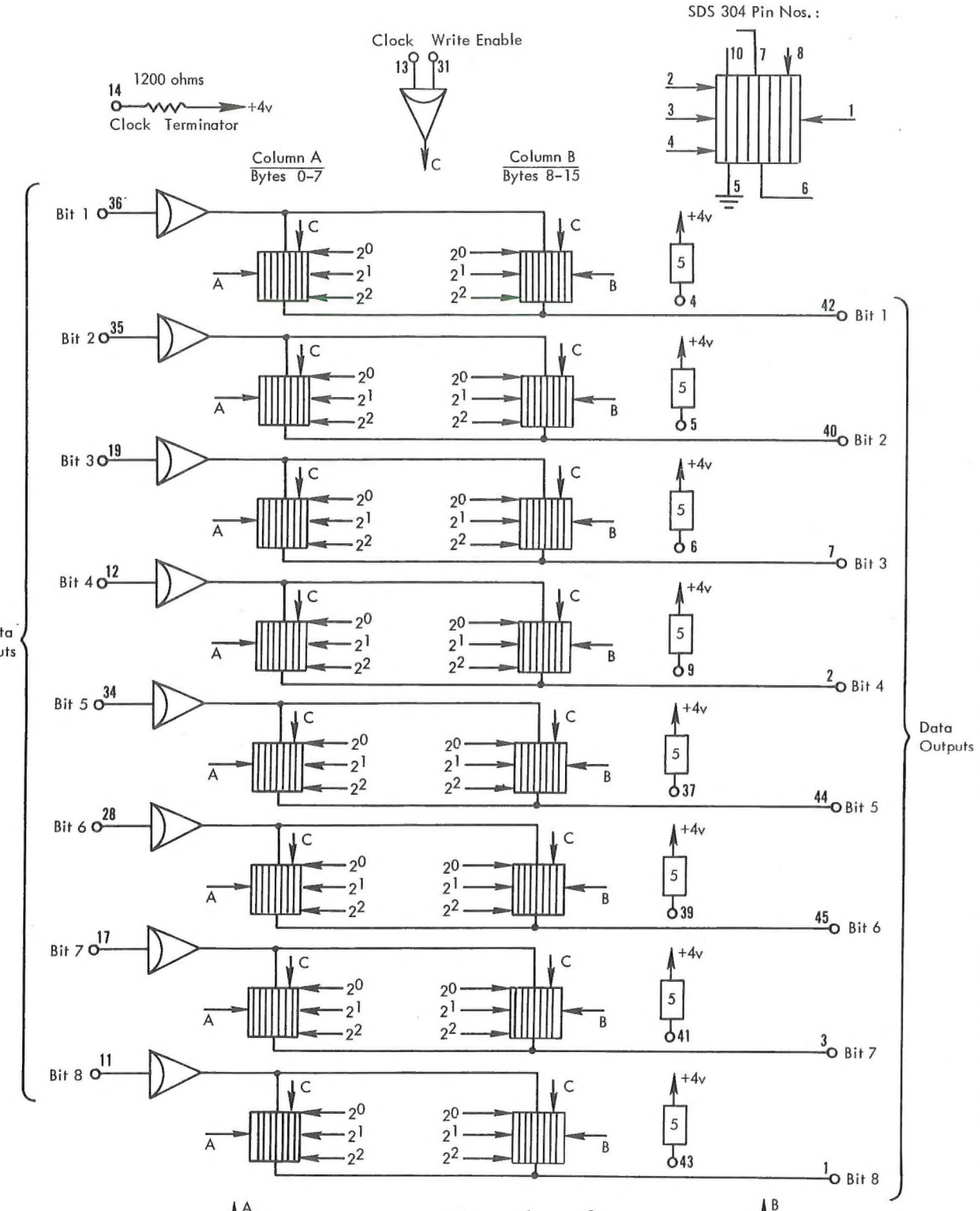
Connection of Pull-up Resistors

The 5-unit-load 220 ohm terminators shown on the logic diagram near the data output pins are used as pull-up resistors for the data output buses. Only one resistor need be connected to one bus, regardless of the number of module outputs connected to that bus. Additional parallel resistors will rob the driver of fan-out, although shortening rise time. If no terminator is connected the circuit cannot operate because there is then no return path to +4 volts. The output circuit of the SDS 304 IC is identical to that of the SDS 306 Buffer.

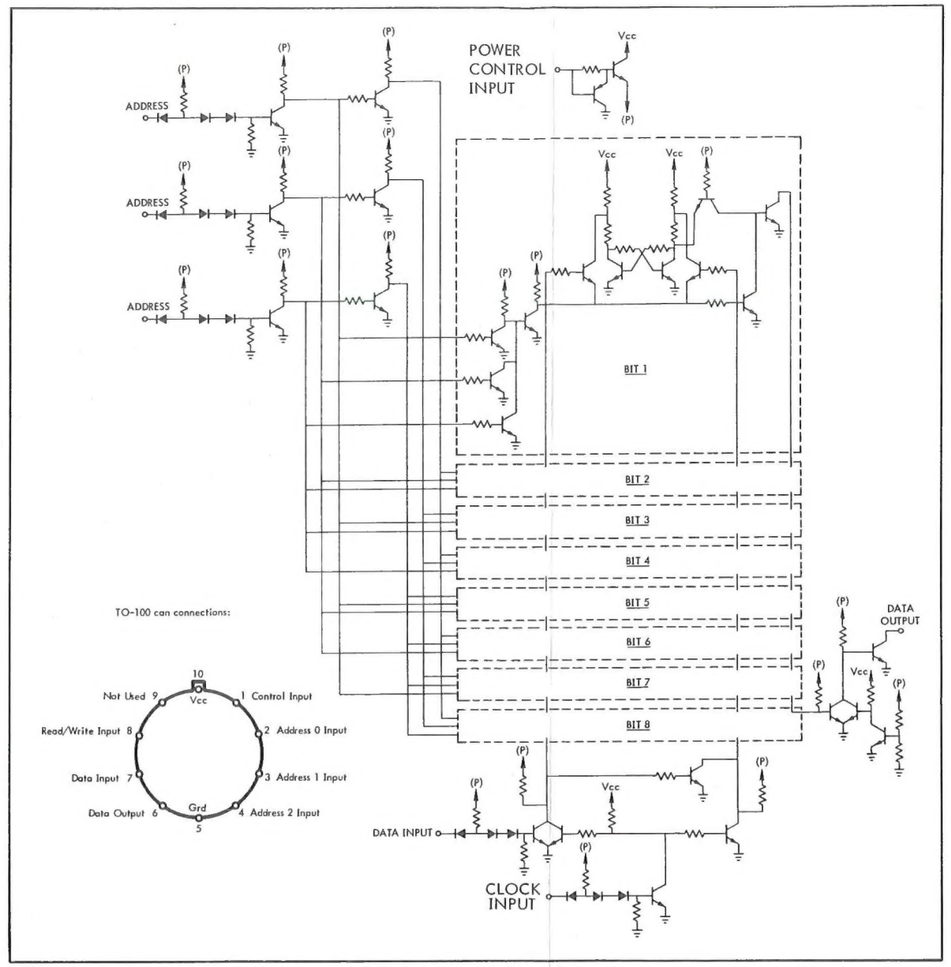


Use of Clock Terminator

The clock terminator is provided for terminating 33 ohm cable when this is used to feed the Clock input. Cable is needed in complex, large scale clock systems. In small-scale systems ordinary logic wiring can be used to route the Clock signal to the module.

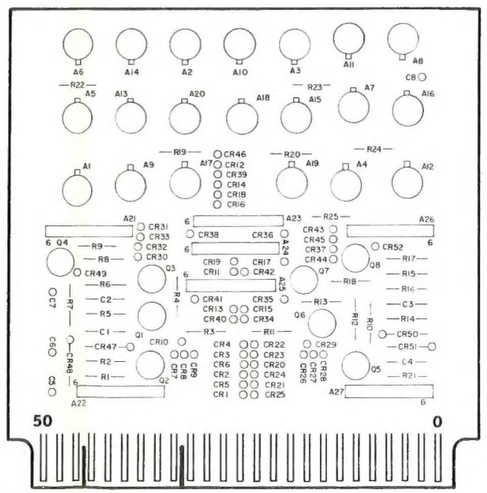


LOGIC DIAGRAM, FT40



SDS 304 Integrated Circuit Schematic

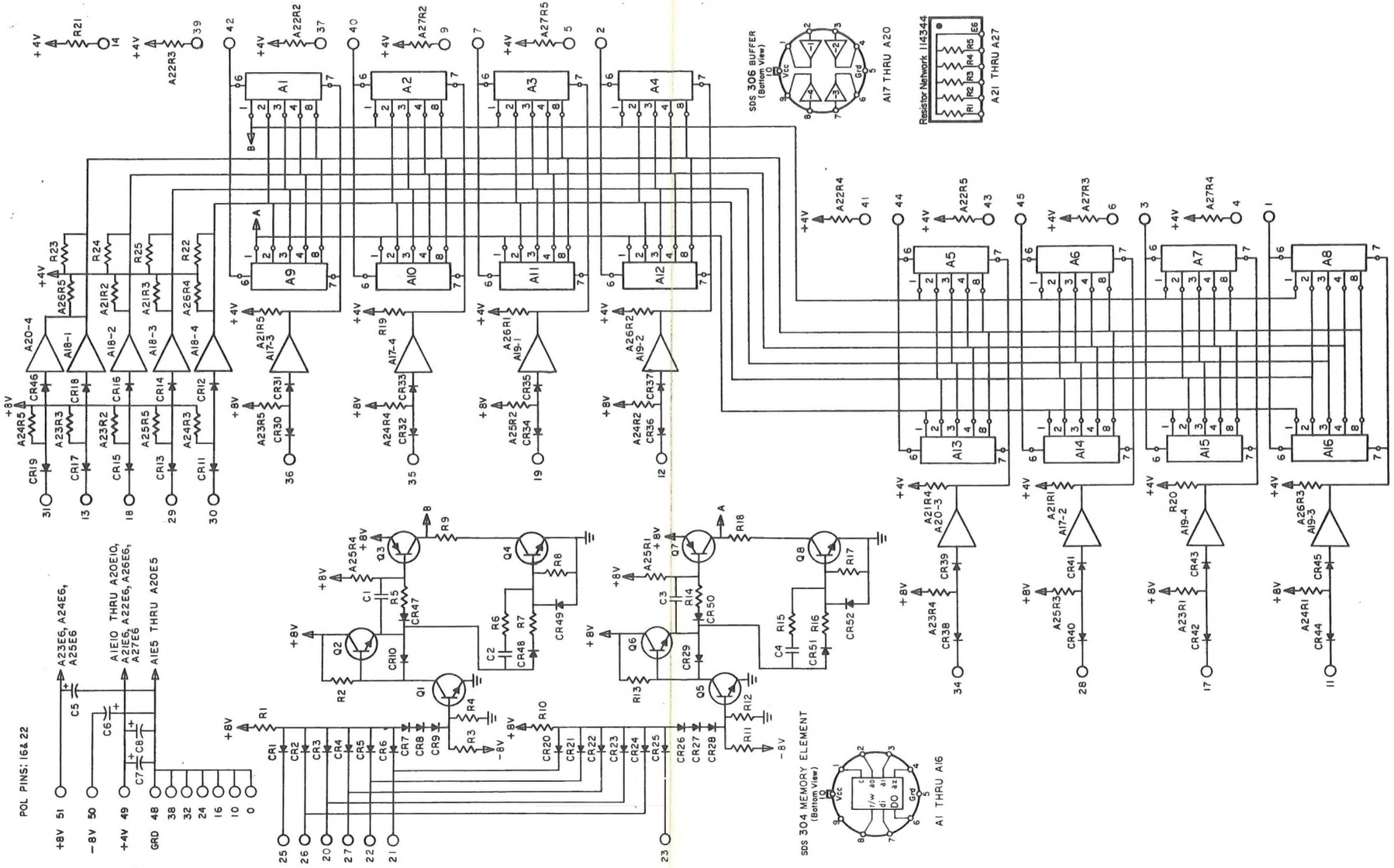
SCREEN



Polarizing Slots 22 16

PARTS LIST

Item		Description	Designator	Qty.
1	Integrated Circuit	SDS 304	A1 thru A16	16
2	Integrated Circuit	SDS 306	A17 thru A20	4
3	Resistor Network	220 ohms, ±5%, 1/4w	A21, A22, A26, A27	4
4	Resistor Network	2.2K, ±5%, 1/4w	A23, A24, A25	3
5	Capacitor, Polystyrene	220 PFD, ±5%, 125v	C1, C3	2
6	Capacitor, Polystyrene	100 PFD, ±5%, 125v	C2, C4	2
7	Capacitor, Tantalum	22 MFD, ±2%, 15vdc	C5, C7, C8	3
8	Capacitor, Tantalum	6.8 MFD, ±2%, 15vdc	C6	1
9	Diode	1N4154	CR1 thru CR46, CR49, CR52	48
10	Diode	1N4157	CR47, CR48, CR50, CR51	4
11	Transistor	2N3013, 2N2369	Q1, Q2, Q4, Q5, Q6, Q8	6
12	Transistor	2N2894	Q3, Q7	2
13	Resistor, Film	1.82K, ±1%, 1/8w	R1, R10	2
14	Resistor, Film	562 ohms, ±1%, 1/8w	R2, R13	2
15	Resistor, Film	10K, ±1%, 1/8w	R3, R4, R11, R12	4
16	Resistor, Film	909 ohms, ±1%, 1/8w	R5, R14	2
17	Resistor, Film	280 ohms, ±1%, 1/8w	R6, R15	2
18	Resistor, Film	221 ohms, ±1%, 1/8w	R19, R20, R22 thru R25	6
19	Resistor, Film	9.1K, ±5%, 1/4w	R7, R16	2
20	Resistor, Film	4.7K ±5%, 1/4w	R8, R17	2
21	Resistor, Film	22 ohms, ±5%, 1/4w	R9, R18	2
22	Resistor, Film	1.2K, ±5%, 1/4w	R21	1



MODEL FT40 SCHEMATIC

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